IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 13, Issue 4, Ver. I (Jul.-Aug. 2018), PP 26-30
www.iosrjournals.org

VCO Based Injection-Locked Clock Multiplier with a Continuous Frequency Tracking Loop

Namitha S N[1], Praveen Kumar Konda[2], Ashwin Kumar[3], Sachin C N Shetty[4]
[1](*M.Tech in VLSI Design and Embedded Systems, Sahyadri College of Engineering and Management, Adyar, Mangaluru, India)*
[2,3,4](*Assistant Professor, Dept. of Electronics and Communication Engg, Sahyadri College of Engineering and Management, Adyar, Mangaluru,*
Corresponding Author:Namitha S N

Abstract :*A phase-locked loop(PLL) is feedback control system that generates a signal that has fixed relation to the phase of reference signal. The PLL responds to both the frequency and the phase of the input signals which automatically raise or lower the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. The wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction. Due to the increase in speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range. Hence there is a necessity of Phase Locked Loop (PLL) which can operate in the GHz range with less lock time. PLL is a mixed signal circuit which involves both digital and analog signal processing units.*

Keywords *-Dividers, Injectionlock, Phase Detector, Voltage-controlled oscillator*

Date of Submission: 09-07-2018 Date of acceptance: 23-07-2018

I. Introduction

VCO based Injection-Locked Clock Multiplier is one of the most promising solutions that can generate low-jitter multi-phase clocks, while costing a limited budget in terms of both area occupation and power consumption. It suffers from minimizing the difference between the free-running frequency of the oscillator and the desired harmonic of the reference source and it also struggles in acquiring an optimal injection position to avoid prominent deterministic jitter. To solve these problems, various continuous frequency tracking techniques have been developed.The most general method is placing the injection-locked oscillator into a phase-locked loop (PLL) to keep its free-running frequency located at the desired harmonic. The mixed signal system has one or more PLL in its block diagram. PLLs are used for tasks like multiplying the clock frequencies, generating clock phases, and generating complex RF modulated signals like phase modulation. Many modern FPGA devices come with integrated PLL to multiply clocks or to adjust the phase of clock outputs. The Modeling of PLLis always difficult because they are part analog and part digital. Circuits that are both analog and digital are called Analog Mixed Signal or AMS. The voltage-controlled oscillator (or VCO), charge pump (or loop amplifier), and loop filter are all analog blocks. The phase detector and dividers are digital blocks. Since the PLL is composed of both analog and digital blocks, it is called mixed signal. PLL is a feedback loop that adjusts the phase and frequency of the VCO to lock to the phase of the input reference oscillator. When the PLL is locked, the output frequency is a fractional multiple of the input frequency.

Fout / N = Fref / R orFout = Fref N / R (1)

II. Architecture

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the changes in the phase that falls in the bandwidth of PLL. The Phase locked loop multiplies a low-frequency reference clock CKref to produce a high-frequency output clock CKout this is known as clock synthesis. The main objective of Phase locked loop is to generate a signal in which the phase is same as the phase of a reference signal. This can be achievedonly after the comparison of the reference and feedback signals. In lock mode, the phase of the reference and feedback signal is zero. The PLL compares two signals but since they are in lock mode, the PLL output is constant. The basic block diagram of PLL is shown in the Fig.1, which consists of five main blocks:

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)

4. Voltage Controlled Oscillator (VCO)
5. Frequency Divider

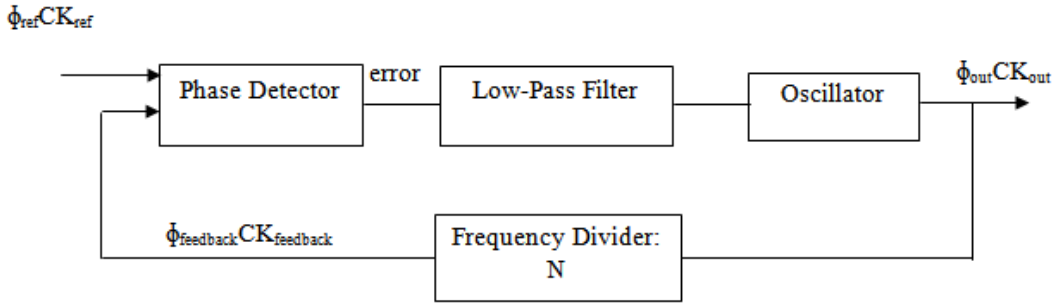

Fig.1: Basic block diagram of a PLL

The Phase Frequency Detector (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock.Depending upon the phase and frequency deviation the signal generates two output signals UP and DOWN. The Charge Pump (CP) is used in PLL to combine both the outputs of the PFD and give a single output. The output of the Charge Pump is fed to a Low Pass Filter (LPF) to generate a DC control voltage. The phase and frequency of the Voltage Controlled Oscillator (VCO) output depends on the generated DC control voltage. If the PFD generates UP signal, then the error voltage at the output of LPF increases which in turn increase the VCO output signal frequency. If DOWN signal is generated, the VCO output signal frequency decreases. The output of VCO is then fed back to the PFD in order to recalculate the phase difference and then the closed loop frequency control system is created.

2.1. PHASE FREQUENCY DETECTOR, CHARGE PUMP AND LOW PASS FILTER:

A typical charge-pump PLL shown in Fig.2 consists of five parts: phase/frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO) and divider.

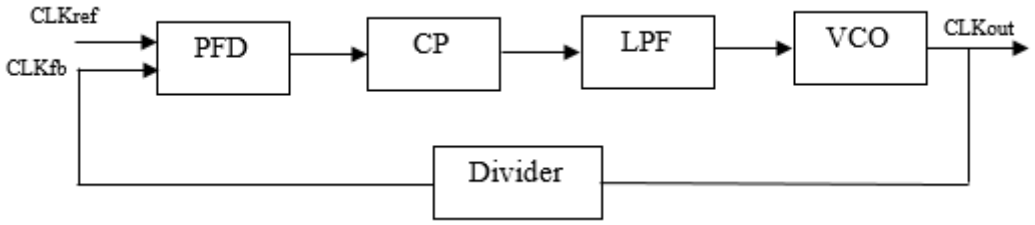

Fig.2: Typical charge-pump PLL

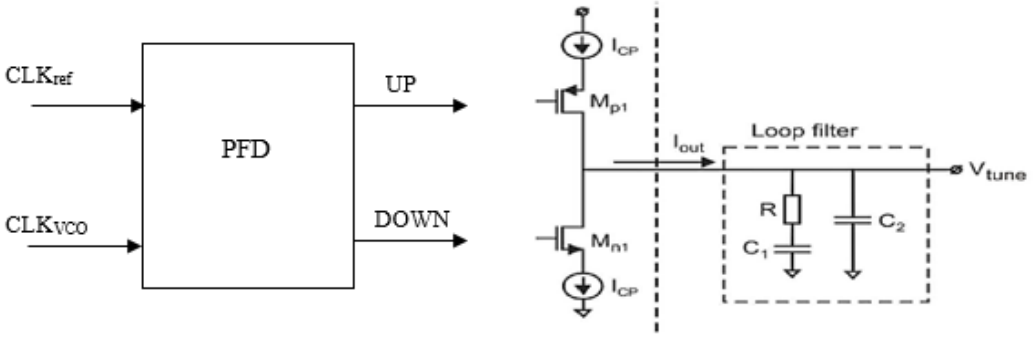

Fig.3: Structure of Phase Frequency Detector, charge pump and loop filter

Phase frequency detector is one of the important parts in PLL circuits. PFD (Phase Frequency Detector) is a circuit that measures the phase and frequency difference between two signals, i.e. the signal that comes from the VCO and the reference signal. The PFD has two outputs UP and DOWN which are signaled according to the phase and frequency difference of the input signals. The output signals of the PFD are fed to the charge pump [1]. The output voltage of the charge pump controls the output frequency of the VCO, so with a change happens at the input of the CP the output voltage will change which will change the output frequency of the VCO and the output of the PFD are connected to gate Mp1 and Mn1, if the frequency of reference clock is larger, the Mp1 will open and the up current source will charge the loop filter. As a result, the tuning voltage Vtune will increase, the VCO output frequency will increase. If the reference frequency is smaller, it will go to the reverse way.

The Open loop transfer function of the second-order CPPLL is given by

$$Y(s) = \frac{I_{cp}}{2\pi}\left(R + \frac{1}{sC}\right)\frac{K_{VCO}}{s}\frac{1}{N} \quad (2)$$

Where $I_{cp}$is current of CP, $K_{vco}$is the gain of VCO (Hz/V), and N is the dividing factor of divider. R and C consist of the one-order LPF. The loop bandwidth describing PLL speed and damping factor describing stability is described as follows,

$$W_n = \sqrt{\frac{I_{cp} K_{VCO}}{2\pi NC}} \quad (3)$$

$$\zeta_n = \frac{R}{2}\sqrt{\frac{I_{cp} K_{VCO}}{2\pi N}}\,C \quad (4)$$

On account of non-ideal effects in PFD and CP, mainly are mismatches between pump currents, the reference spur is given by:

$$Spur(f_{vco} + f_{ref}) = 20\log\left[\frac{K_{VCO} V_m}{2\pi f_{ref}}\right] \quad (5)$$

$V_m$is the peak value of voltage ripple wave determined by mismatch current and impendence of loop filter at reference frequency.

With the reduction in size of CMOS component, the supply voltage and VCO control voltage (V_{ctrl}) from CP get lower. Since PLL output frequency is V_{ctrl} timesK_{vco}, the frequency range is decreased. To provide sufficient frequency range, one simple way is increasingK_{vco}. From equation (3) and (4), we can conclude that largerK_{vco} is good for speed and stability of second-order PLL system. But first K_{vco}cannot be very large, it has an upper limit for the reason CMOS has a saturated area. And more, from equation (5), a larger K_{vco} means larger reference spur. That will decrease frequency accuracy [2].

2.2 VOLTAGE CONTROLLED OSCILLATOR:

An oscillator is an independent system that generates a periodic output without any input signal. VCO is an electronic oscillator designed such that its oscillation frequency is controlled by a voltage input. The frequency of oscillation is controlled by the applied DC voltage, while modulating signals may also be fed into the VCO to cause frequency modulation or phase modulation. The frequency of oscillation must be tunable for the phase of a PLL to be adjustable.

An ideal voltage-controlled oscillator generates a periodic output signal whose frequency is a linear function of control voltage. The output frequency fout can be expressed as;

fout = fnom + gain*Vcont(6)

Where, fnom is a free running frequency, gain is the gain of VCO in Hz/V, and Vcont is a control voltage supplied from charge pump [3].

2.3 Divider:

For clock generation, mostly reference frequencies are limited by the maximum frequency decided by a crystal frequency reference, (mostly in the range of 10 MHz). The divider‘s purpose is to scale down the frequency from the output of the voltage controlled oscillator so that 16 the system can operate at a higher frequency than the reference signal Thus the VCO has to be designed such that the output of VCO is equal to N times the reference frequency. So, the output of the VCO is passed through a divide by N-counter and feedback to the input.

III. Result

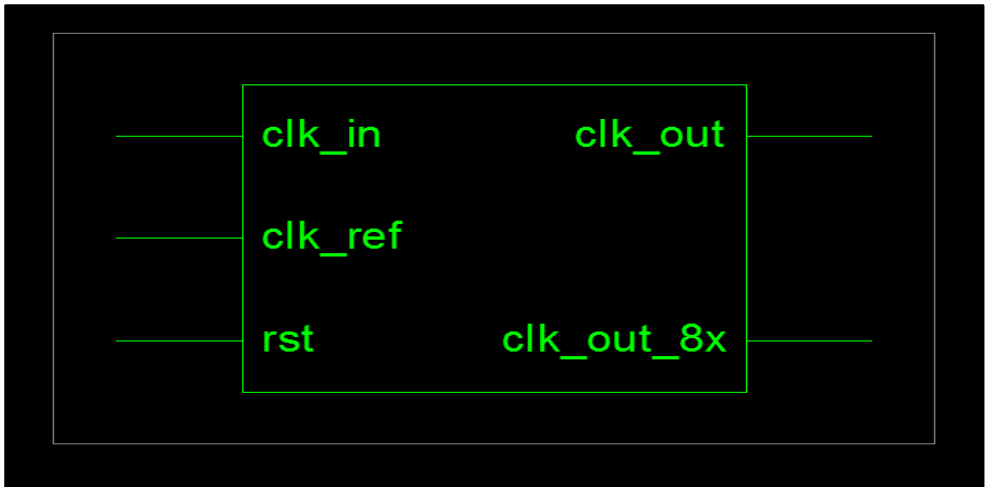

Fig.4: RTL Schematic

```
**************************
Generating Clock Report
**************************

+----------------------+--------------+------+------+------------+--------------+
|         Clock Net    |   Resource   |Locked|Fanout|Net Skew(ns)|Max Delay(ns)|
+----------------------+--------------+------+------+------------+--------------+
|       clk_ref_BUFGP  |  BUFGMUX_X1Y0| No   |   20 |  0.011     |  0.053       |
+----------------------+--------------+------+------+------------+--------------+

* Net Skew is the difference between the minimum and maximum routing
only delays for the net. Note this is different from Clock Skew which
is reported in TRCE timing report. Clock Skew is the difference between
the minimum and maximum path delays which includes logic delays.


   The Delay Summary Report


The NUMBER OF SIGNALS NOT COMPLETELY ROUTED for this design is: 0

   The AVERAGE CONNECTION DELAY for this design is:         0.624
   The MAXIMUM PIN DELAY IS:                                2.153
   The AVERAGE CONNECTION DELAY on the 10 WORST NETS is:    1.326
```

Fig. 5: Place and Route Report

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.2		
Dynamic		0.00	0.00
Quiescent		8.22	9.86
Vccaux	2.5		
Dynamic		0.00	0.00
Quiescent		8.00	20.00
Vcco25	2.5		
Dynamic		0.00	0.00
Quiescent		1.50	3.75
Total Power			33.61

Summary | Power Subtotals | Current Subtotals | Thermal

Fig. 6: Power Analysis

Fig. 4 shows the RTL schematic of PLL.
Fig. 5 shows the place and route report where the maximum delay is 0.053ns and hence frequency is 1.88GHz.
Fig.6 shows the power analysis with total power 33.61mW.

IV. Conclusion

The final simulation result of Low Power Injection-Locked Phase Lock Loop (PLL) is implemented in Xilinx. The current project is later implemented in Cadence. It is capable of producing low-jitter, high-frequency, and full-swing clocks with a high-power efficiency and a small area occupation.

References

[1]. "0.18μm phase / frequency detector and charge pump design for digital video broadcasting for handheld's phase-locked-loop systems "byMhdZaher Al Sabbagh, B.S. The Ohio State University, 2007
[2]. Xuan Ma, and Zongmin Wang, Tieliang Zhang and Song Yang, Beijing Microelectronics Technology Institute. Beijing, China "An Adaptive Wide -Range Phase-Locked Loop",2018 International Conference on Electronics Technology, 978-1-5386-5752-2/18/$31.00 ©2018 IEEE
[3]. "Behavioral Modeling of PLL Using Verilog-A" the simulation standard, July 2003

IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) is UGC approved Journal with Sl. No. 5016, Journal no. 49082.

Namitha S N "Vco Based Injection-Locked Clock Multiplier with a Continuous Frequency Tracking Loop." IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) 13.4 (2018): 26-30.